In the Specification:

On page 1, please replace the paragraph starting at line 18 and ending on page 2, line 3 with the following paragraph:

Fig. 1 shows a typical power LDMOS transistor. A wafer comprises, for example, a p substrate 13 on top of which an epitaxial layer 1 is deposited. This layer 1 includes n conductivity type areas 2 and 4, 15 implanted into the surface to provide a source and drain region, respectively. The epitaxial layer 1 is usually covered with an insulating dielectric layer 7 such as silicon oxide in which a ~~polysilicium~~ polysilicon gate 8 is arranged to cover the channel between the drain 4, 15 and source 2. The drain in this exemplary LDMOS transistor comprises a first region 15 which is n^+ doped and which comprises a connection to a drain electrode 12 arranged above that region 15 through a window in the insulator layer 7. This n^+ region is surrounded by a lighter doped n^- region 4 that extends until under gate 8 to define a channel between the source and the drain region. On the source side of this transistor a p^+ doped sinker 14 is provided which extends from the surface of the epitaxial layer 1 down to the substrate to provide for a backside source contact. Contact 11 connects the source region 2 with the sinker 14.

On page 2, please replace the paragraph starting at line 4 and ending at line 16 with the following paragraph:

Fig. 2 shows an LDMOS transistor as proposed for use, for example, in smart power applications. A wafer comprises, for example, a p substrate 1 which includes n conductivity type areas 2 and 4, 6 diffused or implanted into the surface to provide a source and drain region, respectively. The substrate 1 is usually covered with an insulator layer 7 such as silicon oxide in which a polysilicium gate 8 is arranged to cover the channel between the drain 4, 6 and source 2. Source 2 is coupled with a source electrode 9 through a window in the insulator layer 7. The drain in this exemplary LDMOS transistor comprises a first region 6 which is n^+ doped and which comprises a connection to a drain electrode 10 arranged above that region 6 through a window in the insulator layer 7. From this n^+ region extends a lighter doped n^- region 4 to the left of region 6 until under gate 8 to define a conducting path to the gate channel region. To extend the field effect pinch-off depletion zones from above, a layer of p material 5 is implanted in the upper part of the extended region 4 of the drain and reaching the top surface of the epitaxial layer.

On page 7, please replace the paragraph starting at line 2 and ending at line 15 with the following paragraph:

Turning to the drawings, exemplary embodiments of the present application will now be described. Figure 3 depicts an improved transistor structure according to an exemplary embodiment of the present invention. On top of a p^+ substrate 20, a p epitaxial layer 21 is arranged. For example, the substrate can be doped heavily with $10^{19}/cm^3$ and the epitaxial layer can be less doped with $10^{15}/cm^3$. Along the top surface of the epitaxial layer 21, a source region 23 extends laterally from the source side of gate 26 to an electrically floating electrode or metal interconnection 24. The electrically floating contact 24 connects the oppositely doped source region 23 and a p^+ sinker region 22. The p^+ sinker region 22 reaches from the source region 23 to the p^+ substrate 20. A source metal contact (not shown) is placed along the entire backside of the wafer. Again an insulator layer 25 is placed on the top surface of the epitaxial layer 21 and comprises a gate 26 and windows for respective ~~drain and~~ source and drain electrodes 24, 34. On top of the insulator layer 25, usually a passivation layer (not shown) is deposited.